UNITED STATES PATENT AND TRADEMARK OFFICE

TH

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/632,077	07/31/2003	Gerard Chauvel	TI-35638 (1962-05422)	2220

23494 7590 04/04/2007

TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER	
. HOLLOWAY, DAVID A	
ART UNIT	**PAPER NUMBER**
2109	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/04/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/632,077	CHAUVEL ET AL.	
	Examiner	Art Unit	
	David A. Holloway	2109	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 March 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07/31/2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The numbering of claims is not in accordance with 37 CFR 1.126 which requires the original numbering of the claims to be preserved throughout the prosecution. When claims are canceled, the remaining claims must not be renumbered. When new claims are presented, they must be numbered consecutively beginning with the number next following the highest numbered claims previously presented (whether entered or not). Misnumbered claims 6-20 have been renumbered 5-19.

2. Claims 1-19 are pending in this application and presented for examination.

Objections to the Drawings

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because Fig. 6 includes a reference to "415" which is not mentioned in the specification.

Specification Objections

4. The disclosure is objected to because of the following informalities:

   a. Pages 1-2 of the specification include data that reference copending

applications. These data need to be updated.

b. The 3rd line of [0032] has a spelling error. "one behalf of" should be "on behalf of".

c. "keypad 410" [0042, line 5] should be changed to "keypad 412" to agree with Fig. 6.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claim 1, 2, 13, and 14 are rejected under U.S.C. 35 102(e) as being anticipated by Kramskoy (US Patent # 6,976,254).

7. As to claim 1, Kramskoy discloses a system, comprising: a first processor (Fig. 1, #15); a second processor (Fig. 1, #15a) coupled to the first processor; an

operating system (Fig. 1, #17) that executes exclusively only on the first processor and not on the second processor (Fig. 1) ; and a middle layer software (Fig. 1, #14) running on the first processor and that distributes tasks to run on either or both processors (col. 1, lines 65-67).

8. As to claim 2, Kramskoy discloses the system of claim 1, wherein the middle layer software comprises a Java virtual machine (col 1, line 57).

9. As to claim 13, Kramsky discloses a method (col. 1, lines 65-67) usable in a multiprocessor system, comprising:
executing an operating system (Fig. 1, #17) on only one of a plurality of processors (Fig. 1, #15 and #15a); and distributing tasks to each of the plurality of processors (Fig. 1, #15 and #15a) by middle layer software (Fig. 1, #14) running on the processor (Fig. 1, #15) on which the operating system executes Although the distribution of tasks is not explicitly discussed, it is clear that bytecodes are being executed on both processors (Fig. 1, #15 and #15a, col. 1, lines 56-57). Therefore, tasks are being distributed to both processors.

10. As to claim 14, the claim is rejected for the same reason as claim 2 above.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kramskoy.

13. As to claim 12, Kramskoy does not disclose a programmable task ID register which contains a value indicative of the task currently running on the second processor that is written by the middle layer software running on the first processor. However, a programmable task ID register can be broadly interpreted as a general purpose register of the second processor with a value unique to a task, and a value could be written into that register by middle layer software. It would have been obvious to one skilled in the art at the time of the invention to combine the teachings of Kramskoy with a programmable task ID register, that is written by middle layer software, to make a task specific value, such as the starting address of the code of the second task, available to the task running on the second processor.

14. Claims 3, 4, 5, and 15 are rejected under 35 USC 103(a) as being unpatentable over Kramskoy as applied to claims 1 and 13 above in view of Bolan et al (US Patent 5,210,828), hereinafter Bolan.

15. As to claim 3, Kramskoy does not disclose a synchronization unit coupled to the

first and second processor, said synchronization unit synchronizing the execution of the first and second processors. However, Bolan discloses such a synchronization unit (Fig. 1, #50, the synchronization is done using the interprocessor communications facility).

16. Kramskoy and Bolan are analogous art, because they are both from the same field of endeavor of computer systems.

17. At the time of invention it would have been obvious to one of ordinary skill in the art, having the teachings of Kramskoy and Bolan before him to modify the multiprocessing system of Kramskoy to synchronize the execution of the first and second processors as taught by Bolan. The motivation for doing so would have been to enable the processors to communicate in a fast and efficient manner (Bolan, abstract, lines 8 and 9).

18. As to claim 4, Kramskoy does not disclose a synchronization unit that causes the first processor to transition to a wait mode while the second processor executes a task.

19. However, Bolan discloses a synchronization unit that causes the first processor (Fig. 2, #10) to transition to a wait mode (col. 8, lines 64-88) while the second processor (Fig. 2, #20) executes a task.

20. At the time of invention it would have been obvious to one of ordinary skill in the

art, having the teachings of Kramskoy and Bolan before him to modify the multiprocessing system of Kramskoy to synchronize the execution of the two processors by causing the first processor to transition to a wait mode while the second processor executes a task, as taught by Bolan. The motivation for doing so would have been to allow the hardware accelerator to calculate a result needed by the main processor before the main processor can continue executing its bytecode

21. As to claim 5, Kramskoy does not disclose a synchronization unit that is transitioned from a wait mode to a fully operational mode by a signal being asserted by either the first or second processor to the synchronization unit.

22. However, Bolan discloses a synchronization unit (Fig. 1, #50) that allows the first processor (Fig. 1, #10) to be transitioned from the wait mode (col. 8, lines 64-68) to a fully operational mode (col. 9, lines 39-40) by a signal (col. 9, lines 30-31) asserted from the second processor to the synchronization unit (Fig. 1, #50).

23. At the time of invention it would have been obvious to one of ordinary skill in the art, having the teachings of Kramskoy and Bolan before him to modify the multiprocessing system of Kramskoy to include a synchronization unit that allows the first processor to be transitioned from the wait mode to a fully operational mode by a signal asserted from the second processor to the synchronization unit, as taught by Bolan. The motivation for doing so would have been the motivation used above for claim 4 as well as needing to allow the main processor to resume

processing. It is obvious that one would not want the first processor to remain idle indefinitely.

24. As to claim 15, the claim is rejected for the same reasons as the rejections of claims 4 and 5.

25. Claims 6 and 16 are rejected under 35 USC 103(a) as being unpatentable over Kramskoy as applied to claim 1 above in view of Kikuta et al (US Patent 6,260,131), hereinafter Kikuta.

26. As to claim 6, Kramskoy does not disclose the system of claim 1 further comprising a shared TLB containing a plurality of entries in which virtual-to-physical address translations are stored, each entry also containing a task ID.

27. However, Kikuta discloses a shared TLB containing a plurality of entries in which virtual-to-physical address translations are stored (Fig. 7, "global TLB", col. 3, lines 63-67), each entry also containing a field in which a task ID associated with a task running on the the first or second processor is stored (col. 3, lines 63 to col. 4, lines 1 and 2, the additional information that is generally contained in the page table in order to suppose memory protected, which is also included in the TLB entries stored in the TLB can be unique to a task running on the first or second processor).

28. At the time of invention it would have been obvious to one of ordinary skill in the

art, having the teachings of Kramskoy and Kikuta before him to modify the multiprocessing system of Kramskoy to include a shared TLB as taught by Kikuta. The motivation for doing so would have been to reduce the overhead of the memory manager, since in some cases it will be necessary to update entries in the TLB on all processors instead of just in the shared TLB if each processor has its own TLB. The motivation for TLB entries to also have a task ID would have been to support memory protection that is unique to each task.

29. As to claim 16, the claim is rejected for the same reason as claim 6 above.

30. Claims 7-10 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kramskoy in view of Kikuta as applied to claims 6 and 16 above and further in view of Ara et al (US Pat 5,317,710), hereinafter Ara.

31. As to claim 7, neither Kramskoy nor Kikuta disclose the system of claim 6 wherein the operating system flushes some of the entries in the shared TLB based on task ID.

32. However, Ara discloses a TLB (Fig. 1, #2) that can flush entries based on a task ID (col 1, lines 54-59, here the VMID can be considered a task ID that is associated with a task running on one of the processors). Kikuta discloses that an operating system can control the TLB operations (col. 3,lines 39-40)

33. Kramskoy, Kikuta and Ara are analogous art, because they are all in the same area of endeavor of computer systems.

34. At the time of invention it would have been obvious to one of ordinary skill in the art, having the teachings of Kramskoy, Kikuta, and Ara before him to modify the computer system of Kramskoy and Kikuta to include a shared TLB, wherein an operating system could selectively flushed some of the TLB entries based on the task ID as taught by Ara.

35. The motivation for doing so would have been to allow the system of Kramskoy and Kikuta to efficiently manage address translations based on a task ID (Ara, Fig. 1., contents of VMNR, #1) assigned by the virtual machine.

36. As to claim 8, the claim is rejected for the same reason as claim 7, except that here the middle layer software is flushing the entries instead of the operating system. However, it is well known in the art that middle layer software can perform memory management functions, which would include flushing entries out of a TLB.

37. As to claim 9, the claim is rejected for the same reason as claim 8, since a java virtual machine is simply a type of middle layer software.

38. As to claim 10, the claim is rejected for the same reason as claim 6 above. In addition, if a process identifier is used as the task ID, then the task ID has to be from a process that is running or has run on one of the 2 processors. It is clear that tasks running on different processors will be assigned different process

identifiers.

39. As to claim 17, the claim is rejected for the same reason as claim 7 above.

40. Claims 11 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kramskoy as applied to claims 1 and 13 above in view of Gorgone et al (US 7,137,121), hereinafter Gorgone.

41. As to claim 11, Kramskoy does not disclose the system of claim 1 where the second processor has a programmable context and autonomously switches its own context without support from the operating system executing on the first processor .

42. However, Gorgone discloses the system (Fig. 2) of claim 1 where the second processor (Fig. 2, #44) has a programmable context and autonomously switches its own context (Abstract, lines 2-4) without support from the operating system (Fig. 2, #49) executing on the first processor (Fig. 2, #42).

43. Kramskoy and Gorgone are analogous art, because they are both from the same field of endeavor of computer systems.

44. At the time of invention it would been obvious to one of ordinary skill in the art, having the teachings of Kramskoy and Gorgone before him to modify the computer system of Kramskoy to include the capability of the second processor to autonomously switch its own context without support from the

operating system executing on the first processor as taught by Gorgone.

45. The motivation for doing so would have been to reduce the operating system overhead (Gorgone, abstract, last line).

46. As to claim 18, the claim is rejected for the same reason as claim 11 above.

47. As to claim 19, the claim is analogous to claim 12, except that claim 19 does not restrict the contents of the task ID. Therefore, claim 19 is rejected for the same reasons as claim 12 above.

Conclusion

48. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David A. Holloway whose telephone number is (571)270-1899. The examiner can normally be reached on mon-fri 8:00 am - 5:00 pm (alternate fridays off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nabil El-Hady can be reached on (571)272-3963. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DH 3/16/2007

NABIL M. EL-HADY
SUPERVISORY PATENT EXAMINER